➢ DESCRIPCIÓN EN VHDL – 1 -

1. DESCRIPCION EN VHDL DE UNA AND DE 2 ENTRADAS

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

                ---- Uncomment the following library declaration if instantiating
                ---- any Xilinx primitives in this code.
                --library UNISIM;
                --use UNISIM.VComponents.all;

entity and2e is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC ;
           s : out  STD_LOGIC);
end and2e;

architecture Behavioral of and2e is

begin
s<= a and b;

end Behavioral;
```

2. DESCRIPCION EN VHDL DEL CONTROL PARA LIMPIAPARABRISAS

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

                -- Uncomment the following library declaration if using
                -- arithmetic functions with Signed or Unsigned values
                --use IEEE.NUMERIC_STD.ALL;

                -- Uncomment the following library declaration if instantiating
                -- any Xilinx primitives in this code.
                --library UNISIM;
                --use UNISIM.VComponents.all;

entity limpia is
    Port ( C : in  STD_LOGIC;
           L : in  STD_LOGIC;
           S : in  STD_LOGIC;
           M : out  STD_LOGIC);
end limpia;

architecture Behavioral of limpia is
signal sal1 :STD_LOGIC ;
begin
```

```
sal1 <= not (S) or L;
   M <= sal1 and C;
end Behavioral;
```

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